## ABSTRACT OF THE DISCLOSURE

A vertical double channel silicon-on-insulator (SOI) field-effect-transistor (FET) includes a pair of two vertical semiconductor layers in contact with a pair of parallel shallow trench isolation layers on a substrate, a source, a drain and a channel region on each of the pair of vertical semiconductor layers with corresponding regions on the pair of vertical semiconductor layers facing each other in alignment, a gate oxide on the channel region of both of the pair of the vertical semiconductor layers, and a gate electrode, a source electrode, and a drain electrode electrically connecting the respective regions of the pair of vertical semiconductor layers.